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10/824,504	04/15/2004	Yuichiro Morita	500.40687CX1	6566

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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,504	MORITA ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed August 18, 2006 in response to the Office action dated April 18, 2006. Claims 3 and 5 have been amended. Claims 1-5 are pending in this application.

OBJECTIONS

Specification

1. In view of Applicant's amendment, the objections to the specification have been withdrawn.

Claims

2. In view of Applicant's amendment, the objection to **claim 5** has been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen et al. (U.S. Patent 5,732,236).

5. **As per claim 1**, Nguyen discloses memory controller comprising:

means for receiving, from a processor (col. 2, lines 62-66; col. 3, lines 25-27; Fig. 1, element 10), a request for access to a dynamic random access memory (col. 4, lines 21-26; Fig. 2a, element 38) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *It should be noted that pg. 15, lines 3-5 of Applicant's specification appear to define this means as an "access arbiter." Nguyen's "prioritizer" is equivalent to Applicant's "access arbiter." It should also be noted that even though the "requesting circuits" comprise multiple devices, when all of the multiple devices are taken as a whole they comprise the "microprocessor" (col. 2, lines 62-66), which is in turn a solitary requesting device. Therefore, Nguyen's "microprocessor" is equivalent to Applicant's "processor."*

and memory control means for activating a page to be accessed (col. 5, lines 49-52; col. 3, lines 39-48; Fig. 2b, element 84), based on said access request from said processor (col. 3, lines 27-32 and 55-59), and executing, before a next request for access to a page to be accessed subsequently by said processor, precharge of said page to be accessed subsequently (col. 4, lines 5-13; col. 8, lines 3-11; Fig. 3b). *It should be noted that pg. 30, line 17 – pg. 31, line 5 appear to define this control means a "memory control unit." Nguyen's "plurality of memory bank controllers" is equivalent to Applicant's "memory control unit." It should also be noted that "microprocessor" precharges entire banks using a control line, therefore, it follows that the corresponding*

page within the bank is also precharged. Lastly, please see the italicized citation notes for the limitation above regarding Nguyen's microprocessor.

6. **As per claim 2**, Nguyen discloses memory controller comprising:

means for receiving, from a processor (col. 2, lines 62-66; col. 3, lines 25-27; Fig. 1, element 10), a request for access to a dynamic random access memory (col. 4, lines 21-26; Fig. 2a, element 38) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *Please see the italicized citation notes for the first limitation of claim 1 above.*

and memory control means for activating a page to be accessed (col. 5, lines 49-52; col. 3, lines 39-48; Fig. 2b, element 84), based on said access request from said processor (col. 3, lines 27-32 and 55-59), and executing, before a next request for access to a page to be accessed subsequently by said processor, precharge of a bank corresponding to said page to be accessed subsequently (col. 4, lines 5-13; col. 8, lines 3-11; Fig. 3b). *Please see the italicized citation notes for the second limitation of claim 1 above.*

7. **As per claim 3**, Nguyen discloses a memory controller for use with a processor and a dynamic random access memory, comprising:

a terminal (col. 4, lines 21-26; Fig. 2a, element 38) adapted to receive a request for access from said processor to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *It should be noted that*

Nguyen's "prioritizer" is equivalent to Applicant's "terminal." Also, please see the italicized citation notes for the first limitation of claim 1 above.

and memory control means for issuing an active command for activating a page to be accessed (col. 5, lines 49-52; col. 3, lines 39-48; Fig. 2b, element 84), based on said access request from said processor (col. 3, lines 27-32 and 55-59), and issuing a precharge command for executing, before a next request for access to a page to be accessed subsequently, precharge of said page to be accessed subsequently (col. 4, lines 5-13; col. 8, lines 3-11; Fig. 3b). *It should be noted that in any computer system it is inherently required that a controller/processor issue a "command" in order for any action (such as activating a page or executing a precharge) to be carried out. Also, please see the italicized citation notes for the second limitation of claim 1 above.*

8. **As per claim 4**, Nguyen discloses a memory controller for use with a processor and a dynamic random access memory, comprising:

a terminal (col. 4, lines 21-26; Fig. 2a, element 38) for receiving a request for access from said processor to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *Please see the italicized citation notes for the first limitations of both claim 1 and claim 3 above.*

and memory control means for issuing an active command for activating a page to be accessed (col. 5, lines 49-52; col. 3, lines 39-48; Fig. 2b, element 84), based on said access request from said processor (col. 3, lines 27-32 and 55-59), and issuing a precharge command for executing, before a next request for access to a page to be

accessed subsequently, precharge of a bank corresponding to said page to be accessed subsequently (col. 4, lines 5-13; col. 8, lines 3-11; Fig. 3b). *Please see the italicized citation notes for the second limitations of both claim 1 and claim 3 above.*

9. **As per claim 5**, Nguyen discloses a memory controller comprising:

a terminal (col. 4, lines 21-26; Fig. 2a, element 38) adapted to receive, from a processor, a request for to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *Please see the italicized citation notes for the first limitations of both claim 1 and claim 3 above.*

and a memory control unit adapted to activate a page to be accessed (col. 5, lines 49-52; col. 3, lines 39-48; Fig. 2b, element 84), based on said access request from said processor (col. 3, lines 27-32 and 55-59), and to execute, before a next request for access to a page to be accessed subsequently by said processor, precharge of said page to be accessed subsequently (col. 4, lines 5-13; col. 8, lines 3-11; Fig. 3b). *It should be noted that Nguyen's "plurality of memory bank controllers" is equivalent to Applicant's "memory control unit." Also, please see the italicized citation notes for the second limitation of claim 1 above.*

Response to Arguments

10. Applicant's arguments with respect to **claims 1-5** have been fully considered but they are not persuasive.

11. With respect to Applicant's argument in the first paragraph of page 8 of the communication filed August 18, 2006 that "...it is respectfully submitted that Nguyen fails to teach or suggest the features defined by all of the present claims that precharge of a page to be accessed subsequently is executed before a next request for access to that page takes place", the Examiner respectfully disagrees. Applicant specifically argues that Nguyen activates the precharge for a subsequently accessed page only after receiving the next access request and goes on to state that col. 7, line 45 – col. 8, line 20 of Nguyen clearly shows this situation. However, the Examiner respectfully disagrees and in fact believes that the portion of Nguyen cited by Applicant clearly shows the opposite situation. The Examiner refers Applicant to Nguyen, col. 8, lines 3-11 which states:

> "At time 7330, first bank controller 86 precharges RAS1 to a high logic level and the appropriate page address requested by the subsequent requesting circuit is placed on address bus 22 at time 7335. First bank controller brings RAS1 back to a low logic level and first bank 30 brings the appropriate page address from address bus 22. The memory access for the subsequent requesting circuit begins at time 7335 and ends at 7342."

Therefore, when the secondary address bus is enabled RAS1 is precharged (at time 7330) **before** the page address requested by the subsequent requesting circuit is even placed on the address bus (at time 7335). Accordingly, Nguyen discloses that precharge of a page to be accessed subsequently is executed before a next request for access to that page takes place.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-5** have received a second action on the merits and are subject of a second action final.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
October 30, 2006

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SUPERVISORY PATENT EXAMINER
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